AN10714

Using the BLF574 in the 88 MHz to 108 MHz FM band

Rev. 01 — 26 January 2010 Application note

Document information

Info	Content
Keywords	BLF574, 600 MHz performance, high voltage LDMOS, amplifier implementation, Class-B CW, FM band, pulsed power
Abstract	This application note describes the design and the performance of the BLF574 for Class-B CW and FM type applications in the 88 MHz to 108 MHz frequency range.

Revision history

Rev	Date	Description
01	20100126	Initial version

1. Introduction

The BLF574 is a new, 50 V, push-pull transistor using NXP Semiconductors' 6th generation of high voltage LDMOS technology. The two push-pull sections of the device are completely independent of each other inside the package. The gates of the device are internally protected by the integrated ElectroStatic Discharge (ESD) diode.

The device is unmatched and is designed for use in applications below 600 MHz where very high power and efficiency are required. Typical applications are FM/VHF broadcast, laser or Industrial Scientific and Medical (ISM) applications.

Great care has been taken during the design of the high voltage process to ensure that the device achieves high ruggedness. This is a critical parameter for successful broadcast operations. The device can withstand greater than a 10 : 1 VSWR for all phase angles at full operating power.

Another design goal was to minimize the size of the application circuit. This is important in that it allows amplifier designers to maximize the power in a given amplifier size. The design highlighted in this application note achieves over 600 W in the 88 MHz to 108 MHz band in a space smaller than 50.8 mm × 101.6 mm (2 ” × 4 ”). The circuit only needs to be as wide as the transistor itself, enabling transistor mounting in the final amplifier to be as close as physically possible while still providing adequate room for the circuit implementation.

This application note describes the design and the performance of the BLF574 for Class-B CW and FM type applications in the 88 MHz to 108 MHz frequency band.

2. Circuit diagrams and PCB layout

2.1 Circuit diagrams

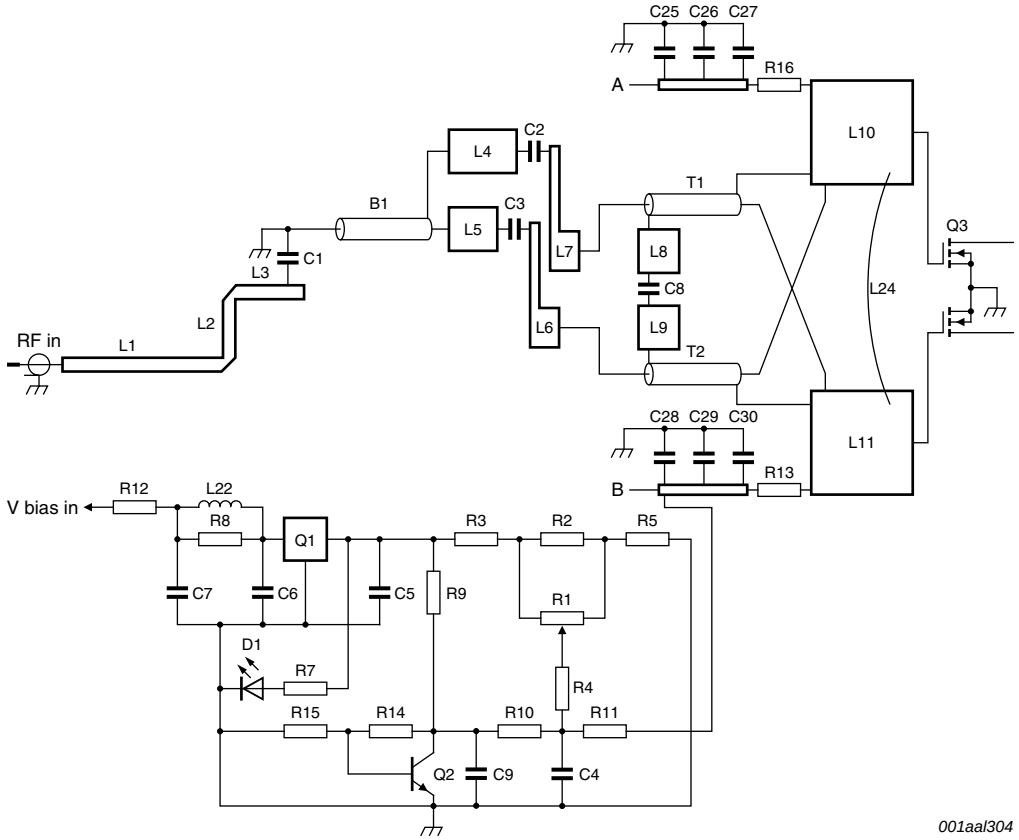


Fig 1. BLF574 input circuit schematic; 88 MHz to 108 MHz

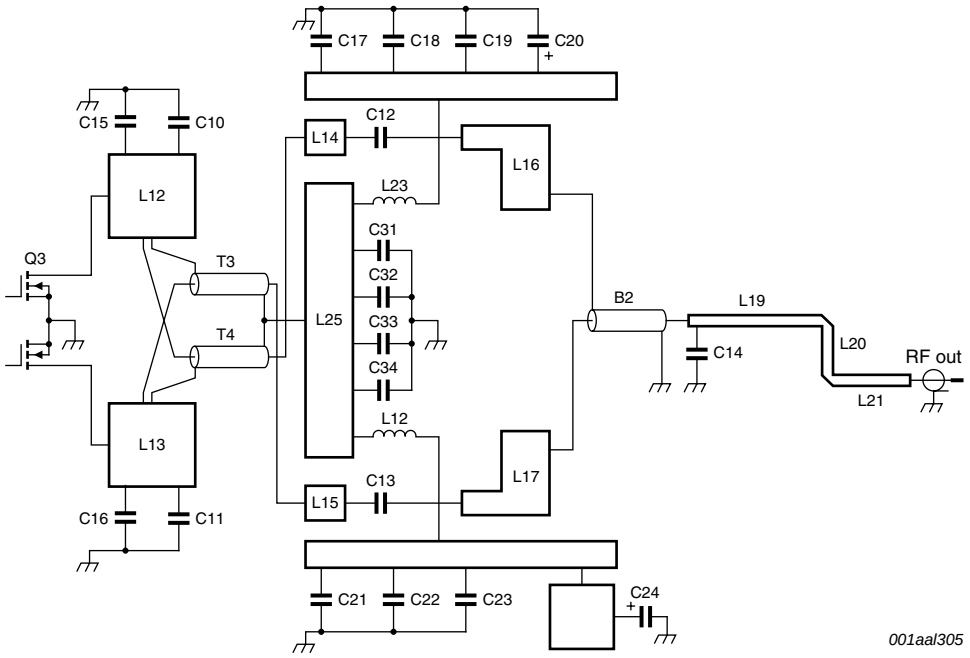
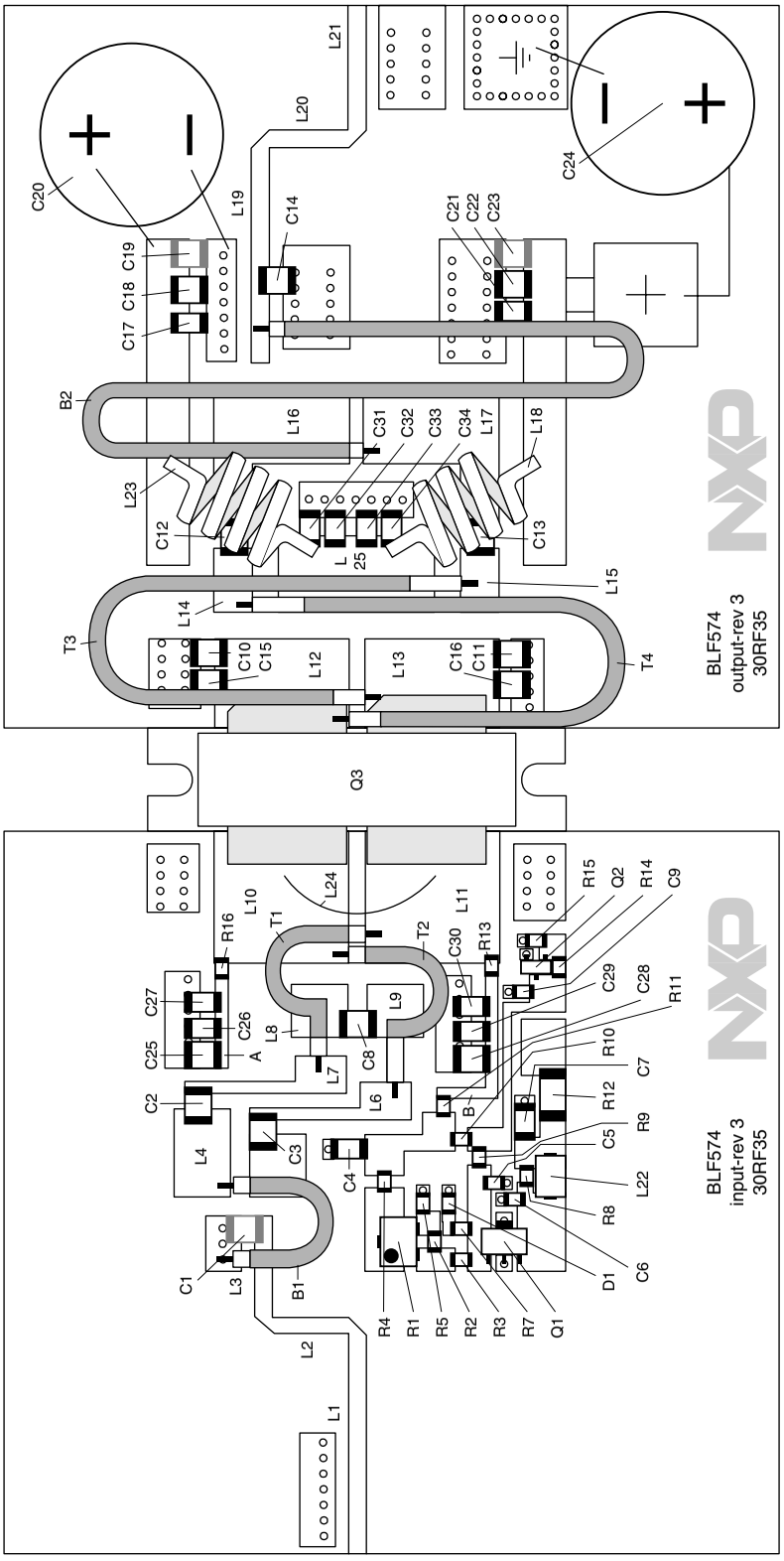


Fig 2. BLF574 output circuit schematic; 88 MHz to 108 MHz

2.2 BLF574 PCB layout



The positions of C1, C19 and C23 are indicated but these capacitors are not connected.

Fig 3. BLF574 PCB layout

2.3 Bill Of Materials

Table 1. Bill of materials for the BLF574 input and output circuits

PCB material: Taconic RF35; ε_r = 3.5; thickness 0.76 mm (30 mil). Figure 3 shows the BLF574 PCB layout.

Designator	Description	Part number	Manufacturer
B1	63.5 mm (2.5 ")/50 Ω semirigid through ferrite[1]	ferrite: BN-61-202	Amidon
		semirigid: 047-50	Micro-Coax
B2	coax cable; 124.5 mm (4.9 ")/50 Ω; ID = 3.5814 mm (0.141 ")	UT-141C-Form-F	Micro-Coax
C1	not connected	-	-
C2, C3	4700 pF ceramic chip capacitor	ATC700B472KW50X	American Technical Ceramics
C4, C7, C26, C29	1 μF ceramic chip capacitor	GRM31MR71H105KA88L	MuRata
C5, C6, C9	100 nF ceramic chip capacitor	GRM21BR71H104KA01L	MuRata
C8	620 pF ceramic chip capacitor	ATC100B621JT100X	American Technical Ceramics
C10, C11	390 pF ceramic chip capacitor	ATC100B220GT500X	American Technical Ceramics
C12, C13	180 pF ceramic chip capacitor	ATC100B181JT200X	American Technical Ceramics
C14	6.8 pF ceramic chip capacitor	ATC100B6R8CT500X	American Technical Ceramics
C15, C16	15 pF ceramic chip capacitor	ATC100B150JT500X	American Technical Ceramics
C17, C21, C31, C32	100 nF/250 V ceramic chip capacitor	GRM32DR72E104KW01L	MuRata
C18, C22, C33, C34	2.2 μF/100 V ceramic chip capacitor	GRM32ER72A225KA35	MuRata
C19, C23	not connected	-	-
C20, C24	1000 μF, 100 V electrolytic capacitor	EEV-TG1V102M	Panasonic
C25, C28	10 nF/35 V ceramic chip capacitor	GRM32ER7YA106KA12L	MuRata
C27, C30	100 nF ceramic chip capacitor	GRM31CR72E104KW03L	MuRata
D1	LED	APT2012CGCK	KingBright
L1	21.7 mm × 1.75 mm (855 mil × 69 mil)	-	-
L2	9.2 mm × 1.65 mm (364 mil × 65 mil)	-	-
L3	9.9 mm × 1.75 mm (390 mil × 69 mil)	-	-
L4, L5	6.2 mm × 5.5 mm (243 mil × 218 mil)	-	-
L6, L7	[2]	-	-
L8, L9	5.2 mm × 5.54 mm (205 mil × 218 mil)	-	-
L10, L11	13.0 mm × 13.2 mm (511 mil × 520 mil)	-	-
L12, L13	8.8 mm × 13.2 mm (345 mil × 520 mil)	-	-
L14, L15	8.83 mm × 3.81 mm (348 mil × 150 mil)	-	-
L16, L17	[2]	-	-
L18, L23	3 turns 14 gauge wire; ID = 7.9 mm (0.310 ")	-	-
L19	21.2 mm × 1.75 mm (834 mil × 69 mil)	-	-
L20	9.5 mm × 1.82 mm (373 mil × 72 mil)	-	-
L21	13.99 mm × 1.7 mm (551 mil × 65 mil)	-	-
L22	ferroxcube bead	2743019447	Fair Rite
L24	50.8 mm (2 "); 14 gauge wire; ID = 15.5 mm (0.61 ")[3]	-	-
L25	7.6 mm × 15.3 mm (299 mil × 604 mil)	-	-

Table 1. Bill of materials for the BLF574 input and output circuits *...continued*

PCB material: Taconic RF35; ε_r = 3.5; thickness 0.76 mm (30 mil). Figure 3 shows the BLF574 PCB layout.

Designator	Description	Part number	Manufacturer
Q1	7808 voltage regulator	NJM#78L08UA-ND	NJR
Q2	SMT 2222 NPN transistor	PMBT2222	NXP Semiconductors
Q3	600 W LDMOST	BLF574	NXP Semiconductors
R1	200 Ω potentiometer	3214W-1-201E	Bourns
R2, R3	432 Ω resistor	CRCW0805432RFKEA	Vishay Dale
R4	2 kΩ resistor	CRCW08052K00FKTA	Vishay Dale
R5	75 Ω resistor	CRCW080575R0FKTA	Vishay Dale
R6	not connected	-	-
R7, R9	1.1 kΩ resistor	CRCW08051K10FKEA	Vishay Dale
R10	11 kΩ resistor	CRCW080511K0FKEA	Vishay Dale
R11	5.1 Ω resistor	CRCW08055R1FKEA	Vishay Dale
R12	499 Ω/0.25 W resistor	CRCW2010499RFKEF	Vishay Dale
R13, R16	9.1 Ω resistor	CRCW08059R09FKEA	Vishay Dale
R14	5.1 kΩ resistor	CRCW08055K10FKTA	Vishay Dale
R15	910 Ω resistor	CRCW0805909RFKTA	Vishay Dale
T1, T2	63.5 mm (2.5 ")/25 Ω semirigid through ferrite[1]	ferrite: BN-61-202	Amidon
		semirigid: 047-25	Micro-Coax
T3, T4	coax cable 86.36 mm (3.4 ")/25 Ω; ID = 2.18 mm (0.086 ")	E22[1]STJ	Thermax

[1] The semirigid cable length is defined in Figure 4.

[2] Contact your local NXP Semiconductors sales person for the artwork file containing the dimensions.

[3] N-male connector mounted as close to the package as possible.

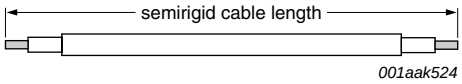


Fig 4. Cable length definition

2.4 PCB form factor

Care has been taken to minimize board space for the design. Figure 5 shows how 600 W can be generated in a space only as wide as the transistor itself.

001aal307

Fig 5. Photograph of the BLF574 circuit board

3. Amplifier design

3.1 Mounting considerations

To ensure good thermal contact, a heatsink compound (such as Dow Corning 340) should be used when mounting the BLF574 in the SOT539A package to the heatsink. Improved thermal contact is obtainable when the devices are soldered on to the heatsink. This lowers the junction temperature at high operating power and results in slightly better performance.

When greasing the part down, care must be taken to ensure that the amount of grease is kept to an absolute minimum. The NXP Semiconductors' website can be consulted for application notes on the recommended mounting procedure for this type of device or from your local NXP salesperson.

3.2 Bias circuit

A temperature compensated bias circuit is used and comprises the following:

An 8 V voltage regulator (Q1) supplies the bias circuit. The temperature sensor (Q2) must be mounted in good thermal contact with the device under test (Q3). The quiescent current is set using a potentiometer (R1). The gate voltage correction is approximately −4.8 mV/°C to −5.0 mV/°C. The V_{GS} range is also reduced using a resistor (R2).

The −2.2 mV/°C at its base is generated by Q2. This is then multiplied by the R14 : R15 ratio for a temperature slope (i.e. approximately −15 mV/°C). The multiplication function provided by the transistor is the reason it is used rather than a diode. A portion of the −15 mV/°C is applied to the potentiometer (R1).

The amount of temperature compensation is set by resistor R4. The ideal value of which proved to be 2 kΩ. The values of R11 and R13 are not important for temperature compensation. However, they are used for baseband stability and to improve IMD asymmetry at lower power levels.

3.3 Amplifier alignment

There are several points in the circuit that allow performance parameters to be readily traded off against one another. In general, the following areas of the circuit have the most impact on the circuit operating frequency and $P_{L(1dB)}$ performance. The modification areas are listed in order of sensitivity, with the most sensitive tuning elements listed first.

Effect of changing the output capacitors (C12 and C13):

- This is a key tuning point in the circuit. This point has the strongest influence on the trade-off between efficiency and linearity.

Effect of the length of the output balun (B2):

- The frequency can be shifted by modifying this element. Typically, the longer the balun, the more the response is shifted to lower frequencies. Conversely, a short balun shifts the response to higher frequencies.

Effect of changing the output 4 : 1 transformers (T3 and T4):

- The frequency can be shifted by modifying these elements. In general, longer transformers shift the whole response to a lower frequency. Shortening the transformers shifts the response to higher frequencies. Changes in efficiency and $P_{L(1dB)}$ is seen when the characteristic impedance of these transformers is changed.

Effect of changing the output capacitor (C14):

- Changing this output capacitor has an effect of tilting the response over the band. The efficiency or $P_{L(1dB)}$ performance can be made more consistent over the band by modifying C14.

Effect of adding capacitance off the drain (C10, C11, C15, and C16):

- A small adjustment in the trade-off between efficiency and $P_{L(1dB)}$ performance can be made by changing these capacitors.

4. RF performance characteristics

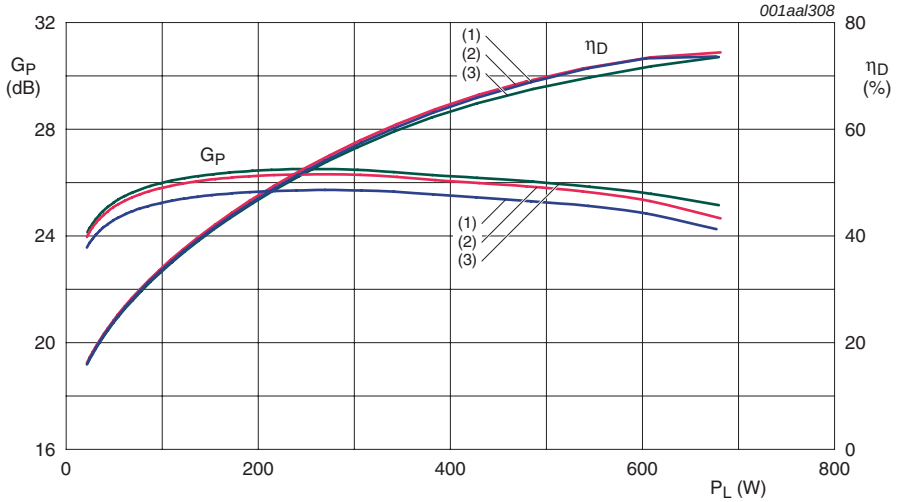
4.1 Continuous wave

Table 2. Class-B performance of the BLF574 at 50 V/600 W

This table summarizes the Class-B performance of the BLF574 at 50 V, I_{Dq} = 200 mA and T_h = 25 °C.

Frequency (MHz)	P_L (W)	G_p (dB)	η (%)	RL (dB)
88	600	24.8	73.3	7.5
98	600	25.3	73.5	9
108	600	25.6	71.9	11.5

4.2 Continuous wave graphics



V_{DD} = 50 V; I_{Dq} = 200 mA.

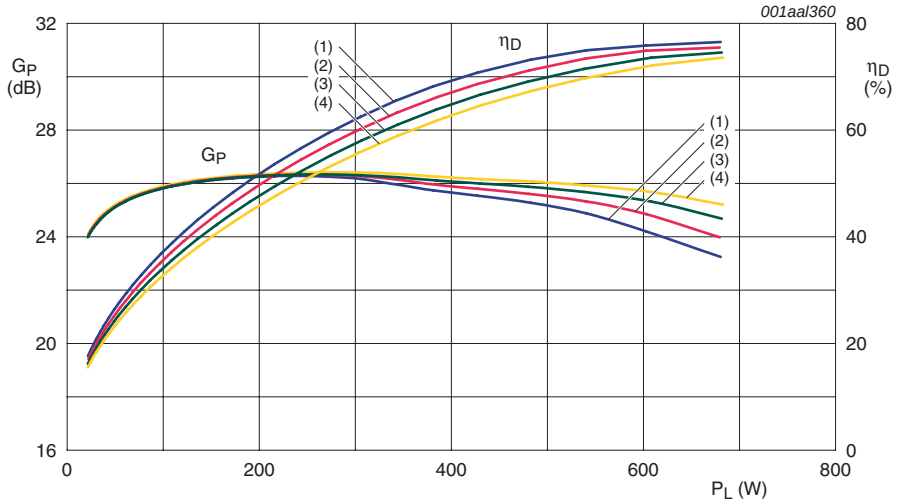
(1) 88 MHz.

(2) 98 MHz.

(3) 108 MHz.

Fig 6. Typical CW data; 88 MHz to 108 MHz

Figure 7 shows the difference in gain and efficiency depending on the drain voltage conditions.



BLF574 at 98 MHz, I_{Dq} = 200 mA.

(1) 46 V.

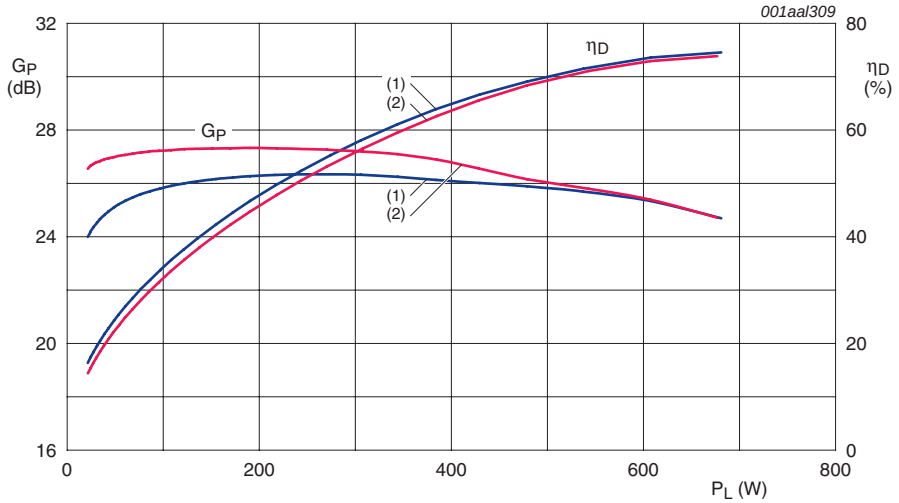
(2) 48 V.

(3) 50 V.

(4) 52 V.

Fig 7. Output gain and efficiency variation under different drain voltage conditions

Figure 8 compares the performance of Class-B and Class-AB amplifier configurations.



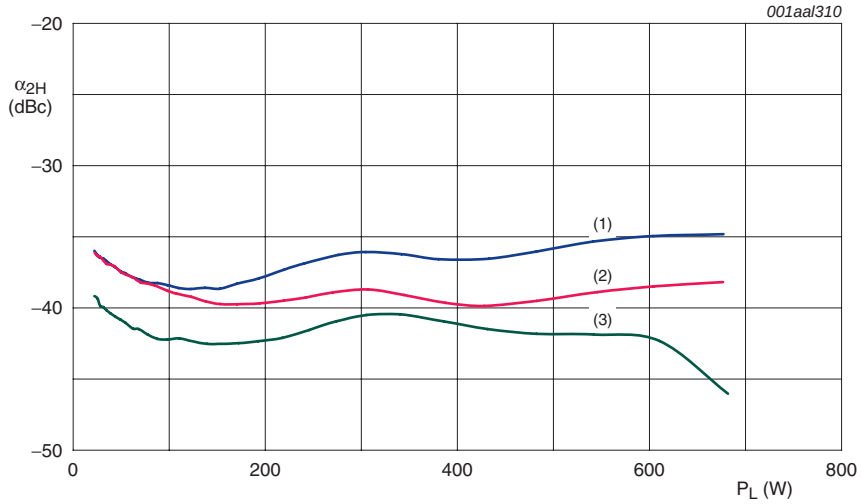
BLF574 at 98 MHz, V_{DD} = 50 V.

(1) 200 mA.

(2) 1 A.

Fig 8. Output gain and efficiency comparison for Class-B and Class-AB amplifiers

Figure 9 shows the second order harmonic performance.



V_{DD} = 50 V; I_{Dq} = 200 mA.

(1) 88 MHz.

(2) 98 MHz.

(3) 108 MHz.

Fig 9. Second order harmonics as a function of output power against frequency

5. Input and output impedance

The BLF574 input and output impedances are given in Table 3. These are generated from a first order equivalent circuit of the device and can be used to get the first-pass matching circuits.

Table 3. Input and output impedance per section

Frequency (MHz)	Input (Z_i)	Output (Z_o)
25	2.020 – j26.216	4.987 – j0.241
50	2.020 – j13.087	4.947 – j0.477
75	2.020 – j8.701	4.882 – j0.705
100	2.020 – j6.500	4.794 – j0.922
125	2.021 – j5.175	4.685 – j1.125
150	2.021 – j4.286	4.559 – j1.310
175	2.022 – j3.647	4.418 – j1.478
200	2.023 – j3.164	4.266 – j1.626
225	2.023 – j2.768	4.106 – j1.755
250	2.024 – j2.480	3.941 – j1.864
275	2.025 – j2.227	3.773 – j1.955
300	2.026 – j2.014	3.605 – j2.028
325	2.028 – j1.832	3.439 – j2.084
350	2.029 – j1.673	3.275 – j2.126
375	2.030 – j1.534	3.116 – j2.154
400	2.032 – j1.410	2.962 – j2.170
425	2.033 – j1.299	2.814 – j2.176
450	2.035 – j1.199	2.673 – j2.172
475	2.037 – j1.108	2.538 – j2.159
500	2.039 – j1.025	2.410 – j2.140

The convention for these impedances is shown in Figure 10. They indicate the impedances looking into half the device.

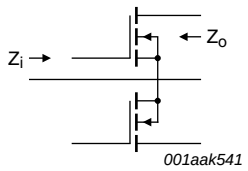
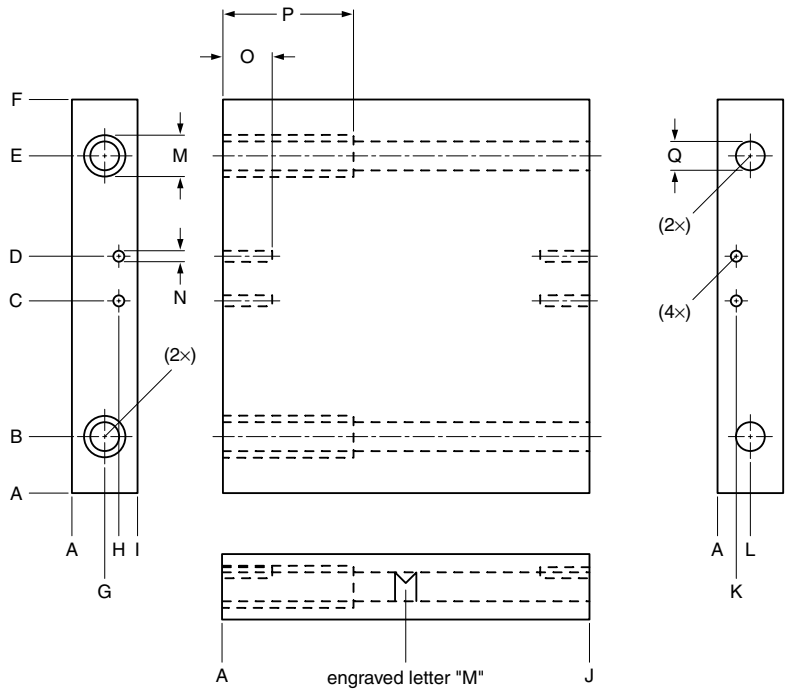


Fig 10. Device impedance convention

6. Base plate drawings

6.1 Input base plate



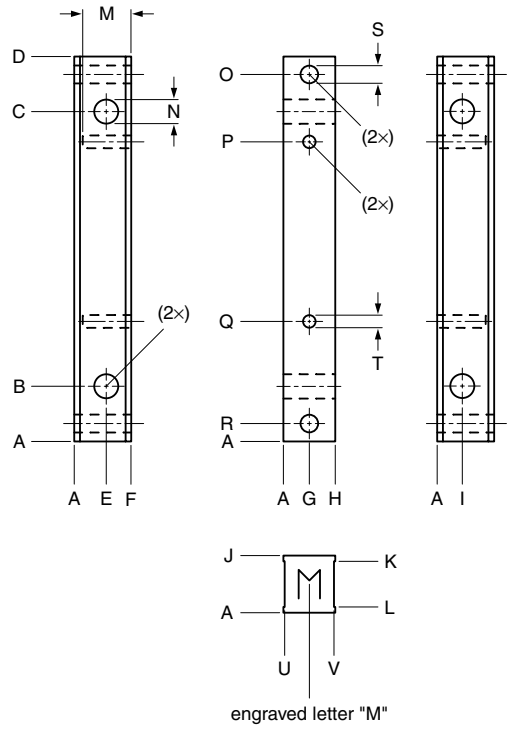
Unit	A	B	C	D	E	F	G	H	I	J	K	L	M	N
mm	0	10.922	37.211	45.847	65.278	76.200	6.350	9.068	12.573	71.120	3.505	6.223	9	M2

Unit	O	P	Q
mm	8	44.32	5.6

001aak566

Fig 11. Input base plate drawing

6.2 Device insert



Unit	A	B	C	D	E	F	G	H	I	J	K	L	M	N
mm	0	10.922	65.278	76.200	6.350	11.328	5.156	10.312	4.978	11.328	10.185	1.143	8	M5[1]

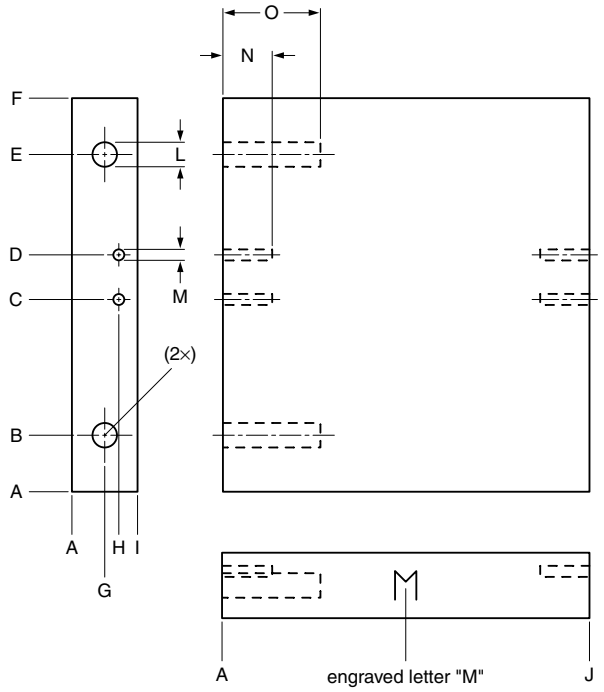
Unit	O	P	Q	R	S	T	U	V
mm	72.644	59.309	23.749	3.556	3.5	M2.5	0.254	10.058

001aak567

(1) +0.5 mm.

Fig 12. Device insert drawing

6.3 Output base plate



Unit	A	B	C	D	E	F	G	H	I	J	K	L	M
mm	0	10.922	37.211	45.847	65.278	76.200	6.350	9.068	12.573	71.120	3.505	M5	M2

Unit	N	O
mm	8	21

001aak568

Fig 13. Output base plate drawing

7. Reliability

Time-to-Failure (TTF) is defined as the expected time elapsed until 0.1 % of the devices of a sample size fail. This is different from Mean-Time-to-Failure (MTBF), where half the devices would have failed and is orders of magnitude are shorter. The predominant failure mode for LDMOS devices is electromigration. The TTF for this mode is primarily dependant on junction temperature (T_j) added to the effect of current density. Once the device junction temperature is measured and in-depth knowledge is obtained of the average operating current for the application, the TTF can be calculated using Figure 14 and the related procedure.

7.1 Calculating TTF

The first step uses the thermal resistance (R_{th}) of the device to calculate the junction temperature. The R_{th} from the junction to the device flange for the BLF574 is 0.25 °C/W. If the device is soldered down to the heatsink, this same value can be used to determine T_j. If the device is greased down to the heatsink, the $R_{th(j-h)}$ value becomes 0.4 °C/W.

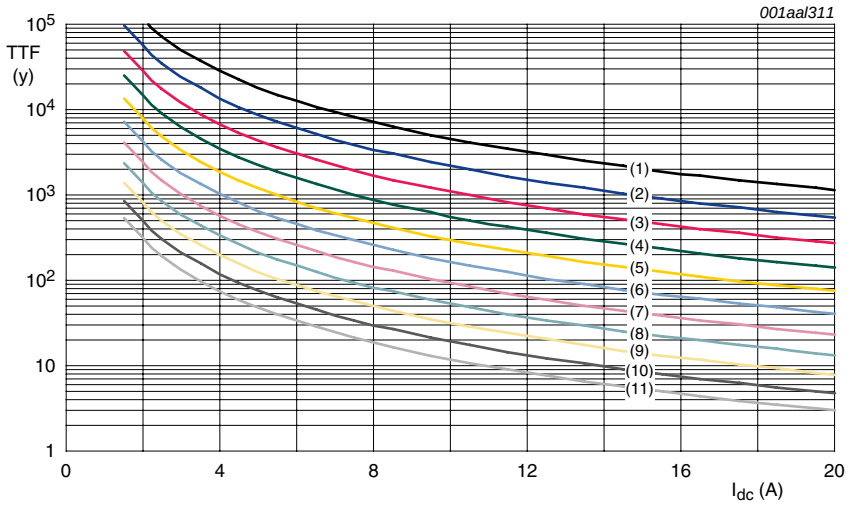
Example: Assuming the device is running at 600 W with the RF output power at 70 % efficiency on a heatsink (e.g. 40 °C). T_j can be determined based on the operating efficiency for the given heatsink temperature:

- Dissipated power (P_d) = 257 W
- Temperature rise (T_r) = $P_d \times R_{th}$ = 257 W × (0.4 °C/W) = 103 °C
- Junction temperature (T_j) = $T_h + T_r$ = 40 °C + 103 °C = 143 °C

Based on this, the TTF can be estimated using a device greased-down heatsink as follows:

- The operating current is just above 17 A
- T_j = 140 °C

The curve in Figure 14 intersects the x-axis at 17 A. At this point, it can be estimated that it would take 100 years for 0.1 % of the devices to fail.



(1) T_j = 100 °C.
(2) T_j = 110 °C.
(3) T_j = 120 °C.
(4) T_j = 130 °C.
(5) T_j = 140 °C.
(6) T_j = 150 °C.
(7) T_j = 160 °C.
(8) T_j = 170 °C.
(9) T_j = 180 °C.
(10) T_j = 190 °C.
(11) T_j = 200 °C.

Fig 14. BLF574 time-to-failure

8. Test configuration block diagram

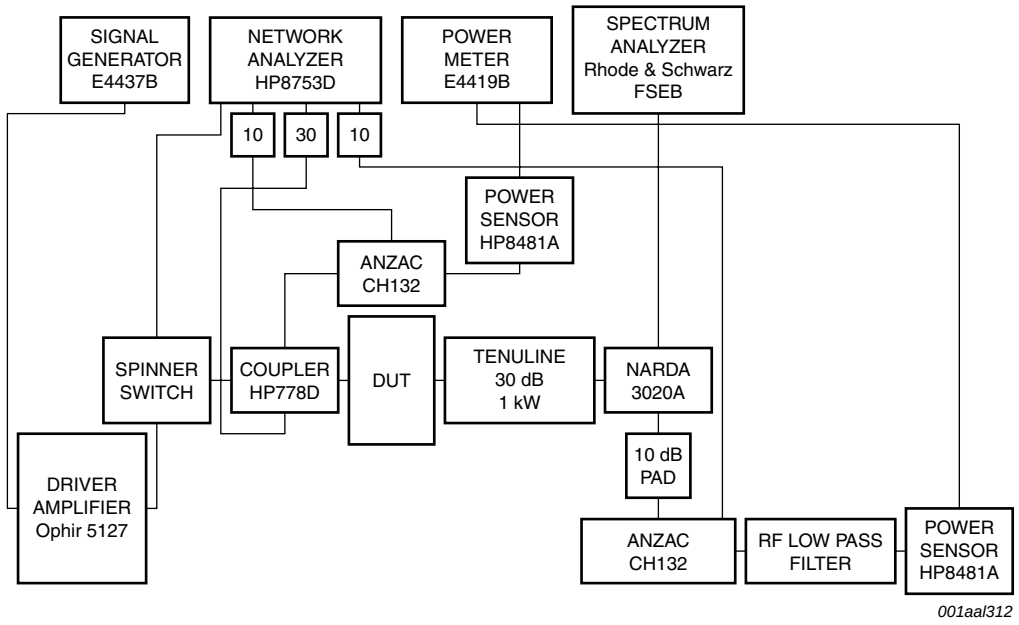


Fig 15. BLF574 test configuration

9. PCB layout diagrams

Please contact your local NXP Semiconductors' salesperson for copies of the PCB layout files.

10. Abbreviations

Table 4. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
IMD	InterModulation Distortion
IRL	Input Return Loss
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PCB	Printed-Circuit Board
SMT	Surface Mount Technology
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

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13. Contents

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